What is claimed is:

1. A semiconductor device, comprising

a substrate;

an active area formed within the substrate;

a first non-planar metallization level which is formed on the substrate and is in contact with the active area; and

a second planar metallization level arranged spaced apart from the first metallization level above the substrate and connected to the first metallization level via a through connection.

2. The semiconductor device according to claim 1, wherein the semiconductor device includes a field effect transistor having a gate, a source area and a drain area, wherein the first non-planar metallization level includes a first portion connected to the source area, a second portion connected to the drain area and a third portion at least partially covering the gate, and wherein the second planar metallization level includes at least one portion connected to the first portion of the first non-planar metallization level or to the second portion of the first non-planar metallization level.

3. The semiconductor device according to claim 2, wherein the first portion and the third portion of the first non-planar metallization level are connected.

4. The semiconductor device according to claim 2, wherein between the first non-planar metallization level and the second planar metallization level an insulating layer is arranged, wherein in the insulating layer at

least one through connection for a connection of the first non-planar metallization level to the second planar metallization level is formed.

5. The semiconductor device according to claim 2, wherein the third portion is implemented to shield the gate against electrostatic or electrodynamic interferences.

6. An amplifier circuit comprising a field effect transistor according to claim 2.